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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,501	10/24/2003	David Walter Flynn	550-466	7230
23117 7590 03/21/2007 NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			EXAMINER DINH, NGOC V	
			ART UNIT	PAPER NUMBER
			2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/691,501

Applicant(s)

FLYNN ET AL.

Examiner

NGOC V. DINH

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

FINAL REJECTION

1. This Office Action is responsive to Amendment filed 01/23/2007. Claim 1 is amended.

The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

2. Applicant's arguments have been fully considered but are not persuasive.

In the remarks, applicants argue in substance that:

- a) "connecting the bus 100 to the memory via SCAN_PATH".
- b) "Scan_Path does not transfer multi-bit data words (parallel transfer).
- c) "using the scan path during normal processing operation.

The Examiner respectfully submits that applicant's position is misplaced:

a) There is not mention in claim 1 the limitation "via SCAN_PATH". Claim 1 only cites "a system bus coupled to said circuit and said memory", and this limitation is clearly taught by Godfrey fig. 2-3 as cited in section 3 of the examiner previous office action.

Assuming Applicant's argument "connecting the bus 100 to the memory via SCAN_PATH" be in the claim, and this limitation is also taught by Godfrey: "an internal bus 100 coupling ... and registers", col. 3/67 to col. 4/1; and these registers are formed a SCAN_PATH ; "scan cells contains shift register elements that connect together to form a scan path", col. 2/14-18; and these register (Scan_Path) further coupled to FIFO in fig. 3. Furthermore in col. 10/claim 15, Godfrey teaches this limitation as [the scan path is in accordance with IEEE 1149.1 bus standard]

b) Godfrey clearly teaches Scan path transfer multi-bit data words [Parallel stages, col. 5/22-25; col. 8/ 12-13; 34-35.

c) Godfrey clearly teaches this limitation as in col. 2/18-20.

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Accordingly, the rejections are respectfully maintained and incorporated by reference as set forth in the last office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-7, 9, 11-12, 13-19, 21, 23-24 are rejected under 35 U.S.C.102 (e) as being anticipated by Godfrey PN 6,550,031.

Godfrey teaches:

Per claims 1 and 13, apparatus for processing data [microcontroller, col. 3, lines 25-30; fig. 1], comprising:

a circuit used in processing data [fig. 2, col. 4, lines 48-65], said circuit having one or more nodes [peripheral registers, 104a-b, 120a-b, 108a-b, ... fig. 2; plurality of miscellaneous logic, col. 9, claim 1] for storing one or more data values that together define a state of said circuit [col. 1, lines 55-62; configuration state of peripheral, col. 5, lines 8-25];

a memory for storing data 200, fig. 2];

a multi-bit wide system bus [bus 100, fig. 2; bus 100 connected to memory 200 via scan-path, col. 5, lines 8-10, 27-35; fig. 3; since the SCAN_PATH supports parallel processing as mentioned above, thus the system bus 100 also supports multi-bits parallel processing] coupled to said circuit and said memory and operable to transfer multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory [col. 3, line 65 to col.4, line 5]; and

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a state saving controller [trigger, col. 3, lines 11-20; col. 8, lines 29-40; The microcontroller of claim 1 further comprising a trigger applied to each of the scan cells, col. 10/claim 5] coupled to said circuit and said system bus and operable in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes [col. 8, lines 54-60] and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words [col. 1, lines 55-65; SAVE/RESTORE col. 3, lines 50-60; col. 6, lines 30-40; col. 9, lines 12-35].

Per claims 2 and 14, circuit is a processor core [124, fig. 2; col. 4, lines 9-12; circuit not only storing data but also processes data/instruction].

Per claims 3 and 15, one or more nodes are each coupled to a respective scan chain cell [col. 2, lines 16-18, 28-32; col. 2, lines 55-65] within said circuit, said state saving controller being operable in response to said state saving trigger [col. 3, lines 11-20; col. 8, lines 29-45] to store said data values within respective scan chain cells [col. 9, scan cells, claim 1; fig. 8, trigger with scan cells] and to serially read [read out serially, col. 2, lines 20-32] said data values from said scan chain cells to form said one or more state saving multi-bit data words [col. 3, lines 37-38, fig. 5 with plural stages of scan cells for saving data; col. 2, lines 29-32, 65-67; col. 3, lines 1-5; col. 9, lines 1-10].

Per claims 4 and 16, a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains [col. 2, lines 22-25, boundary scan chain] operating in parallel [serialization of parallel data, col. 5/20-25; col. 8/12-20 to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read [scan hardware, col. 4/38-40; col. 2/14-32].

Per claims 5 and 17, scan chain cells are also operable to perform test functions upon said circuit [JTAG test, col. 44-45; col. 9/12-25, debug system].

Per claims 6 and 18, circuit is a further memory and said data values are bits of data words stored in said further memory [each element in fig. 2 is either a register or latch which stores bits of data, fig. 3; fig. 7; col. 5/27-35].

Per claims 7 and 19, memory is coupled to a built-in self-test controller operable to perform self-test operations [JTAG test, col. 44-45; col. 9/12-25, debug system] upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words [col. 6, lines 44-62; col. 9, lines 1-20].

Per claims 9 and 21, state saving controller is operable in response to a state restoring trigger [trigger, col. 3/11-20; SAVE/RESTORE, col. 3/53-55] to generate a sequence of memory read requests [scan-read, col. 7/30-35] on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby **restore** [*multiple snapshots*, col. 2/62-65; *snapshots*, col. 9/26-28] said state of said circuit [col. 3/53-55; col. 9/13-20, debug system].

Per claims 11 and 23, wherein said state saving trigger comprises execution of a state saving program instruction [col. 8, lines 29-40].

Per claims 12 and 24, state saving trigger comprises initiation of a diagnostic test upon said circuit [col. 2, lines 14-29].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject

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matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 8 and 20 are rejected under 35 U.S.C 103(a) as being unpatentable over Godfrey.

Per claims 8 and 20, Godfrey does not teach data burst mode transfer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include burst mode transfer into Godfrey system to improve speed of data transmission because burst mode data transmission is a well-known method for data transfer wherein burst mode enable to transfer group of memory words as a page of data, this speed up data transfer (as evidenced by Bissessur et al. PN 6,807,600, col. 5/45-50].

5. Claims 10 and 22 are rejected under 35 U.S.C 103(a) as being unpatentable over Godfrey, and in view of Borden PN 5,790,561.

Per claims 10 and 22, Godfrey does not teach multi-bit state saving data words is stored in a user specified region of said memory.

Borden teaches a boundary-scan cells test using a user register [30, fig. 2; col. 3, lines 40-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Borden 's teaching into Godfrey's system in order to implement special user functions [col. 3, lines 45-48].

Conclusion

6. ***THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).***

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191.

The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned are (571)-273-8300 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

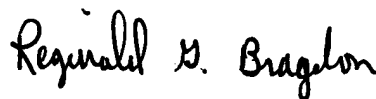


NGOC DINH

Patent Examiner

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March 12, 2007



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